

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method comprising:

supplying a negative voltage to at least one deselected wordline of a non-volatile memory array from a decoder coupled to the at least one deselected wordline during a programming operation on a selected wordline;

providing the negative voltage and a control negative voltage to the decoder; and

supplying a positive voltage to [[a]] the selected wordline of the non-volatile memory array to program the selected wordline while supplying the negative voltage.

Claim 2 (canceled)

Claim 3 (previously presented): The method of claim 1, further comprising supplying the negative voltage to all wordlines of the non-volatile memory array except the selected wordline.

Claim 4 (previously presented): The method of claim 1, further comprising providing a second positive voltage signal to a selected bitline of the non-volatile memory array.

Claim 5 (previously presented): The method of claim 4, further comprising reducing a leakage current through at least one deselected cell coupled to the selected bitline of the non-volatile memory array while programming the selected wordline, wherein the at least one deselected cell comprises a multi-level cell of a flash memory.

Claim 6 (canceled)

Claim 7 (previously presented): The method of claim 1, further comprising providing the control negative voltage to a substrate of a transistor of the decoder coupled to pass the negative voltage to the at least one deselected wordline.

Claim 8 (canceled)

Claim 9 (previously presented): The method of claim 1, further comprising supplying the negative voltage to the deselected wordline during a first time period, and

supplying a positive voltage to the same wordline during a second time period to program at least one memory cell coupled thereto.

Claim 10 (currently amended): An apparatus comprising:

a decoder to supply a negative voltage to a deselected address line of a memory array, the decoder comprising a first transistor of a first polarity coupled to receive a negative control voltage and the negative voltage and to pass the negative voltage to the deselected address line, and a second transistor of a second polarity coupled to the first transistor and the deselected address line to pass a program pulse to the deselected address line if it becomes a selected address line, the decoder further comprising a pre-driver circuit to control an intermediate node coupled to a gate terminal of the first transistor and a gate terminal of the second transistor.

Claim 11 (original): The apparatus of claim 10, wherein the decoder is further coupled to supply a positive voltage to the same address line if it is selected to be programmed.

Claims 12 – 13 (canceled)

Claim 14 (currently amended): The apparatus of claim 10, wherein the further comprising a pre-driver circuit is to disable the first transistor if the deselected address line becomes a selected address line.

Claim 15 (original): The apparatus of claim 10, further comprising a plurality of memory cells coupled to the decoder via the deselected address line.

Claim 16 (original): The apparatus of claim 15, wherein the plurality of memory cells comprise multi-level cells of a flash memory.

Claim 17 (currently amended): An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

supply a negative voltage to at least one deselected wordline of a memory array; and

provide a negative control voltage to a substrate of a transistor coupled to pass the negative voltage to the at least one deselected wordline;

supply a positive voltage to a selected wordline of the memory array to program the selected wordline while the negative voltage is supplied to the at least one deselected wordline;
and

control a first pre-driver circuit coupled to the at least one deselected wordline to pass a positive control voltage to a first control node coupled to a first pair of transistors of different polarities, and to control a second pre-driver circuit coupled to the selected wordline to discharge a second control node coupled to a second pair of transistors of different polarities.

Claim 18 (cancel).

Claim 19 (currently amended): The article of claim [[18]] 17, further comprising instructions that if executed enable the system to supply the negative voltage to all wordlines of the memory array except the selected wordline.

Claim 20 -21 (canceled)

Claim 22 (previously presented): A system comprising:

a nonvolatile memory array having a plurality of memory cells each coupled to a wordline and a bitline;

a decoder coupled to the nonvolatile memory array to supply a negative voltage to a deselected wordline of the nonvolatile memory array, wherein the decoder comprises a first transistor of a first polarity to pass the negative voltage to the deselected wordline and a second transistor of a second polarity coupled to the first transistor to pass a program voltage, if the deselected wordline becomes a selected wordline; and

a wireless interface coupled to the nonvolatile memory array.

Claim 23 (original): The system of claim 22, wherein the decoder is further coupled to supply a positive voltage to the deselected wordline if it becomes a selected wordline.

Claim 24 (original): The system of claim 22, further comprising a second decoder to supply a positive voltage to a selected wordline while the negative voltage is supplied to the deselected wordline.

Claim 25 (previously presented): The system of claim 22, wherein the first transistor comprises a well coupled to receive a negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected wordline.

Claim 26 (canceled)

Claim 27 (previously presented): The system of claim 22, further comprising a pre-driver circuit to disable the first transistor if the deselected wordline becomes a selected wordline, wherein the pre-driver circuit comprises a transistor chain coupled to an intermediate node coupled to a gate terminal of the first transistor, wherein the transistor chain is to provide a ground potential to the intermediate node to disable the first transistor.

Claim 28 (previously presented): The system of claim 22, wherein the nonvolatile memory array comprises a flash memory.

Claim 29 (original): The system of claim 28, wherein the flash memory comprises a multi-level cell flash memory.

Claim 30 (original): The system of claim 22, wherein the wireless interface comprises an antenna.

Claim 31 (previously presented): The apparatus of claim 10, wherein the first transistor comprises a well coupled to receive the negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected address line.

Claim 32 (previously presented): The system of claim 22, further comprising a negative switch coupled to provide the negative voltage and a negative control voltage to the decoder.

Claim 33 (currently amended): The system of claim 32, wherein the negative switch is coupled to further provide the negative voltage and the negative control voltage to a second decoder coupled to another wordline of the non-volatile memory array.

Claim 34 (cancel)

Claim 35 (currently amended): The apparatus of claim [[34]] 10, wherein the pre-driver circuit further comprises a transistor chain to provide a ground potential to the intermediate node if the deselected address line is selected to be programmed.

Claim 36 (previously presented): The apparatus of claim 35, wherein the transistor chain comprises a plurality of series-coupled transistors of the first polarity having a top transistor having a first terminal coupled to the intermediate node, the first terminal further coupled to a first terminal of a third transistor of the second polarity.

Claim 37 (cancel)

Claim 38 (new): The article of claim 17, further comprising instructions that if executed enable the system to supply the negative voltage to the deselected wordline during a first time period, and supply the positive voltage to the same wordline during a second time period to program at least one memory cell coupled thereto.